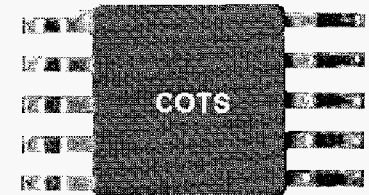
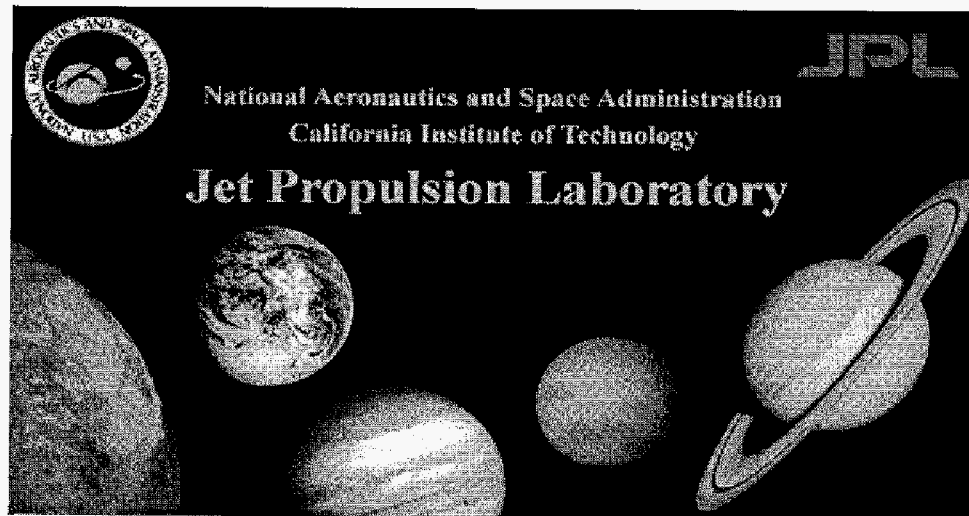
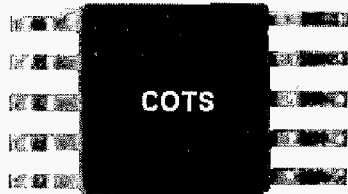


# Commercialization of Military & Space Electronics - Conference

February 12-15, 2001

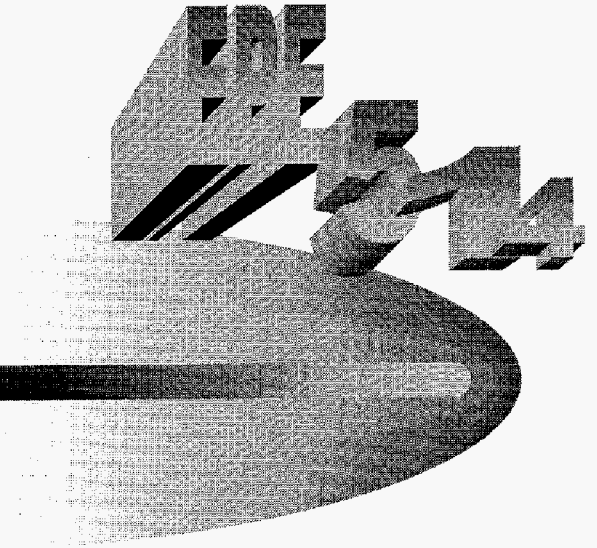
**Commercial Off-The-Shelf (COTS) Program**  
Using Nondestructive Methods (C-SAM) for COTS  
PEMs Screening and Qualification



**Mike Sandor, Shri Agarwal**  
4800 Oak Grove Drive  
Pasadena, CA 91109

**Phone: (818) 354-0681 FAX: (818) 393-4559**

**JET PROPULSION LABORATORY**  
**Electronic Parts Engineering Office**



---

**AGENDA:**

**C-SAM Inspection**

**Failure Mechanisms/Studies**

**C-SAM Screening Method**

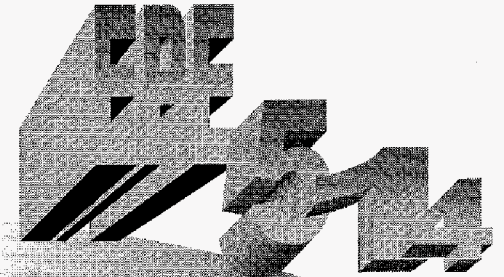
**Test Data**

**Reject Criteria/Failure Analysis**

**Other Work**

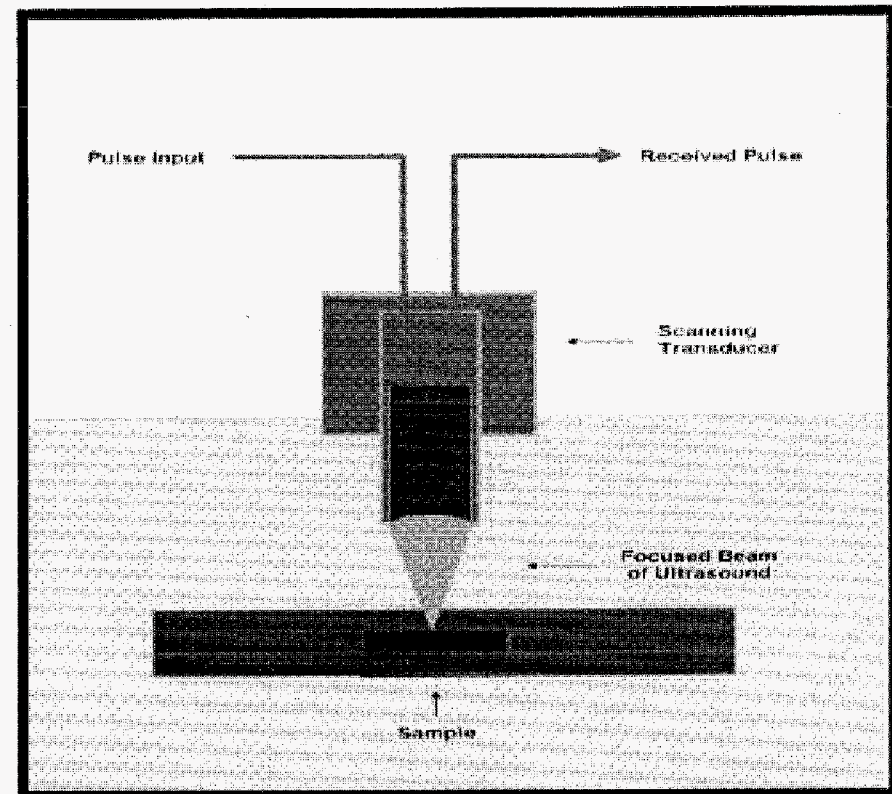
**Summary**

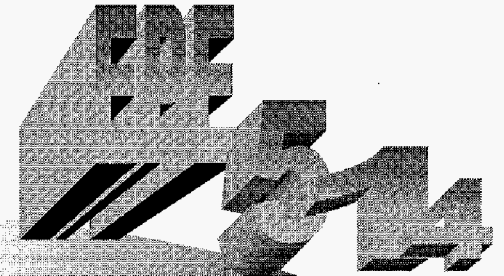
The work was performed at Jet Propulsion Laboratory California Institute of Technology under contract to the National Aeronautics and Space Administration



## C-SAM Inspection Characteristics:

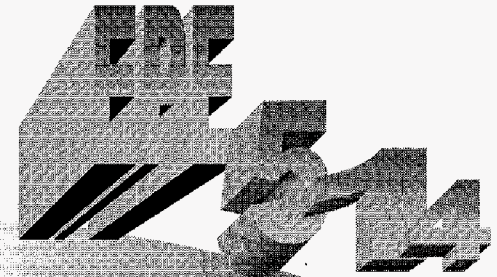
- Nondestructive Method
- Ultrasound Signal
- Ceramics, Plastics, Metals
- Voids, Cracks, Delamination, Anomalies, Defects, Disbonds
- Relatively inexpensive
- Cheap Reliability Insurance





## **Possible Failure Mechanisms from PEM Delamination Based on Independent Studies:**

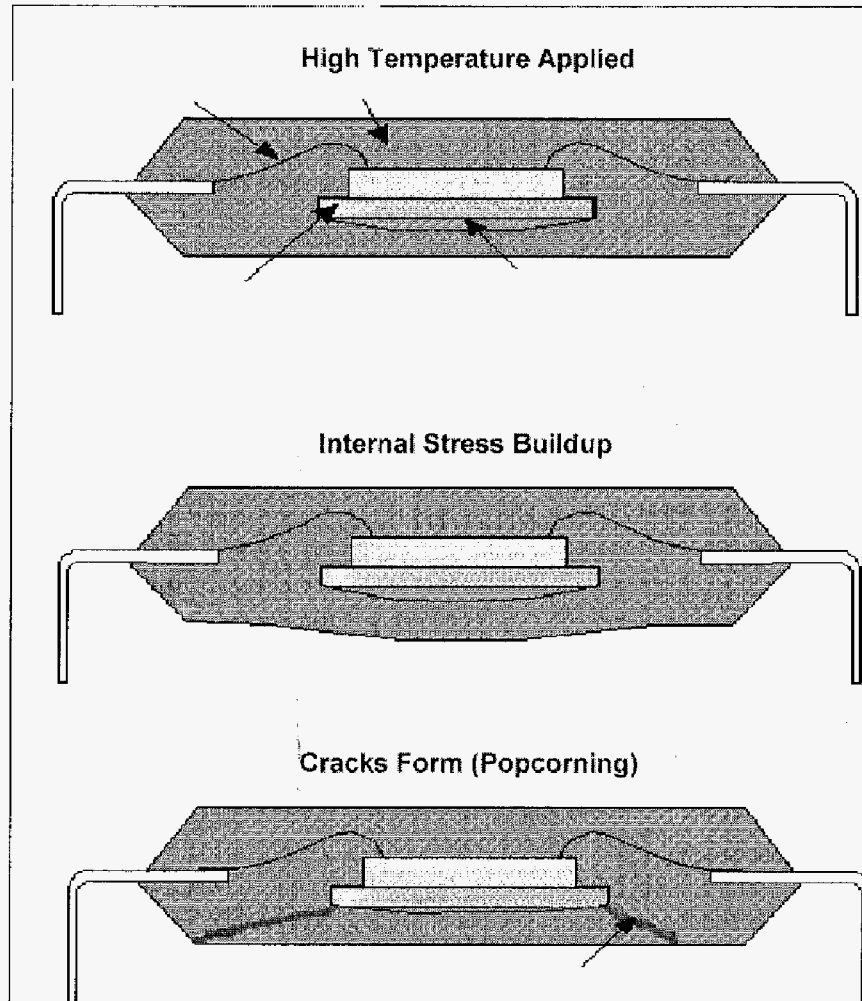
- **Stress-induced passivation damage over the die surface**
- **Wire bond degradation due to shear displacement**
- **Accelerated metal corrosion**
- **Die attach adhesion**
- **Intermittent electricals at high temperature**
- **Popcorn cracking**
- **Die cracking**



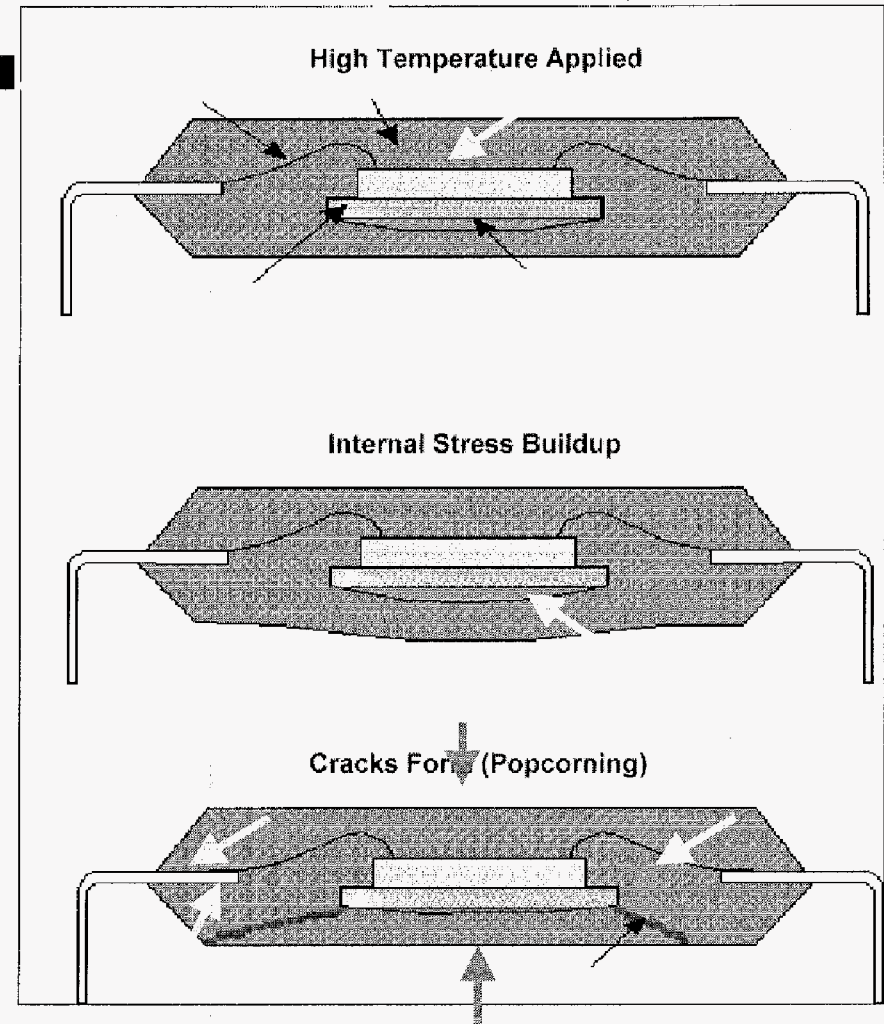
## **Eight Independent Studies on C-SAM Delamination /Reliability:**

- Failure Criteria for Inspection Using Acoustic Microscopy After Moisture Sensitivity Testing of Plastic Surface Mount Devices; Alcatel Bell, Texas Instruments, Philips Semiconductor
- A Case Study of Plastic Part Delamination; ITT Aerospace/Communications
- The Application of Scanning Acoustic Microscopy to Control Moisture/Thermal Induced Package Defects; Texas Instruments
- C-SAM Analysis of Plastic Packages to Resolve Bonding Failure Mode Miscorrelations; Texas Instruments
- On the Role of Adhesion in Plastic Packaged Chips Under Thermal Cycling Stress; Siemens
- Relation Between Delamination and Temperature Cycling Induced Failures in Plastic Packaged Devices
- Correlation of Surface Mount Plastic Package Reliability Testing to Nondestructive Inspection by Scanning Acoustic Microscopy; Texas Instruments
- The Mystery of the Cracked Dice; Analog Devices

# Popcorning Failure Mechanism from Internal Moisture

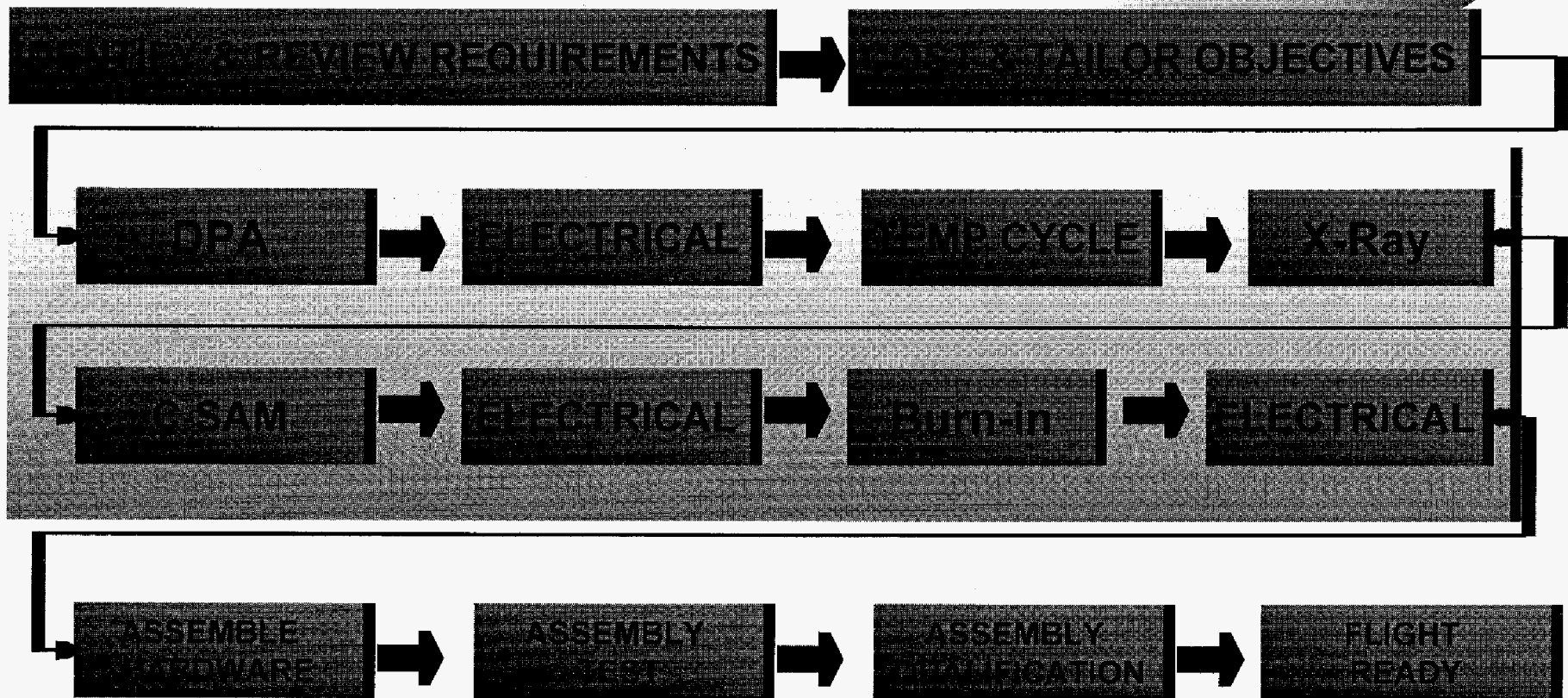


# C-SAM Inspection Points for delamination



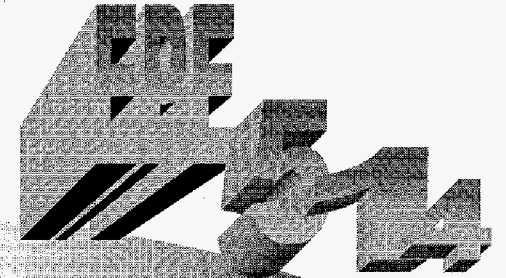
**JET PROPULSION LABORATORY**  
**Electronic Parts Engineering Office**

**C-SAM is Included in JPL's**  
**Full Part Level Screening**



**COTS<sup>++</sup> Plastic Infusion Critical Screening Flow**  
**(Tailored for Project application/mission requirements)**

**JET PROPULSION LABORATORY**  
**Electronic Parts Engineering Office**



## **COTS<sup>++</sup> Upscreening Rejects by Part Type & Vendor**

	<u>Amplifier- A</u>	<u>ADC- B</u>	<u>ADC2-B</u>	<u>DC-DC Con.-C</u>	<u>Voltage C-A</u>	<u>S.Regulator-B</u>
DPA:	0/4	1/8	TBD	0/4	0/4	0/4
Incoming:	0/78	n/a	4/79	1/78	0/80	8/80
<b>C-SAM:</b>	<b>3/78</b>	<b>38/78</b>	<b>9/75</b>	<b>16/77</b>	<b>5/80</b>	<b>0/80</b>
Temp Cycle:	0/78	10/78	0/75	3/77	0/80	3/72
Burn-In:	0/78	3/68	0/75	0/74	0/80	9/69
QCI:	0/10	0/10	0/10	0/10	0/10	0/10
Total:	3/78	51/78	TBD	20/78	5/80	20/80

**JET PROPULSION LABORATORY**  
**Electronic Parts Engineering Office**



**LOT by LOT Test Results:**

**CSAM Yields**  
**06/12/2000**

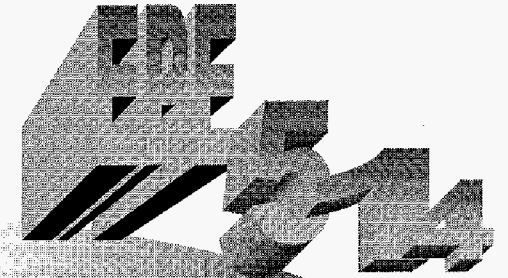
<b>Part Type</b>	<b>Manufacturer</b>	<b>Yield</b>
NPN Transistor 1	A	83%
Switching Diode	A	0%
NPN Transistor 2	A	100%
Zener Diode	A	50%
NPN Transistor 3	A	100%
Op-Amp 1	B	87%
Op-Amp 2	C	0%
Op-Amp 3	C	7%
Phase Detector	D	100%
MMIC	E	40%

**Results are**  
**package/ vendor**  
**assembly dependent.**

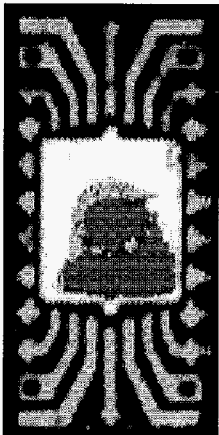
**Failed lots were**  
**replaced and retested.**

Lot sizes range  
from 15-30 parts each.

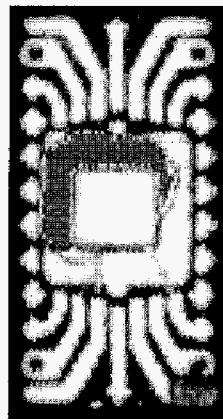
**JET PROPULSION LABORATORY**  
**Electronic Parts Engineering Office**



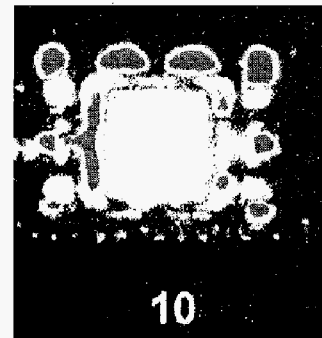
**C-SAM Rejects (JPL examples):** (Devices with  $>> 10\%$  delamination in critical areas are suspect and are rejected)



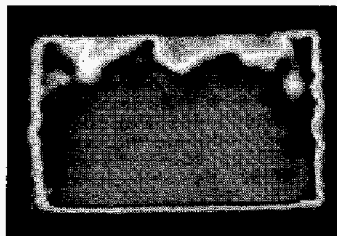
Reject



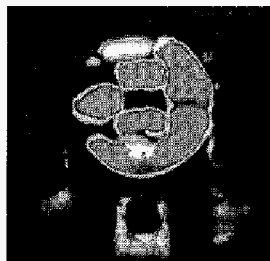
Reject



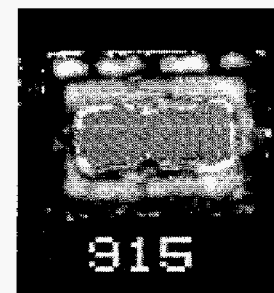
Reject



Reject



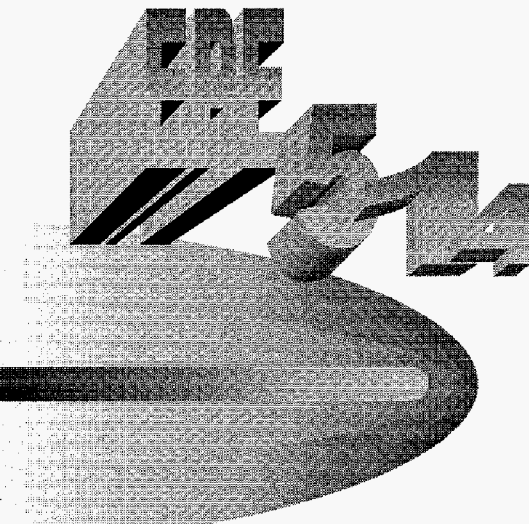
Reject



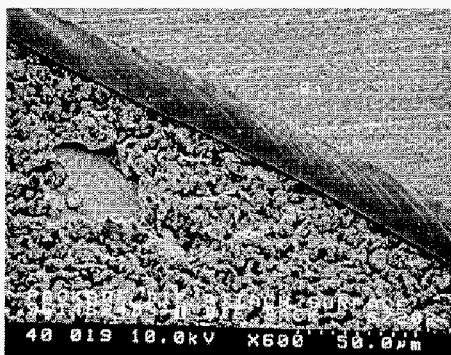
Pass\*

\*Delamination is not evident because of die top coating used by the manufacturer

**JET PROPULSION LABORATORY**  
**Electronic Parts Engineering Office**



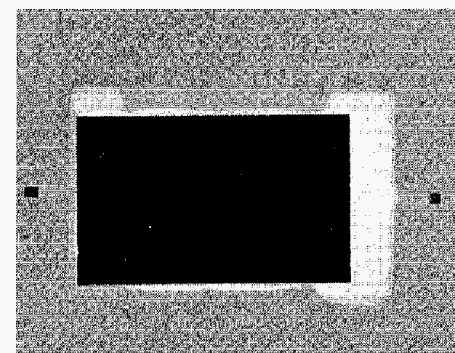
**C-SAM Delaminations Confirmed by Failure Analysis: (JPL examples):**



A. Die attach void at  
the heat sink surface



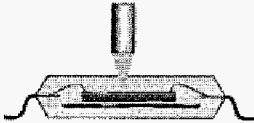
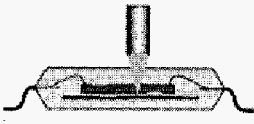
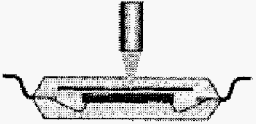
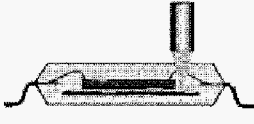
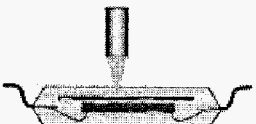
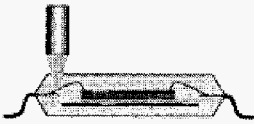

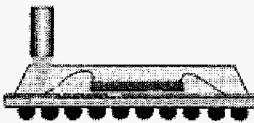

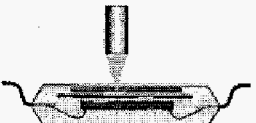
B. Bubble exists from  
Mylar tape near pin 5



C. Delamination and lack  
of adhesion between  
die and heat sink

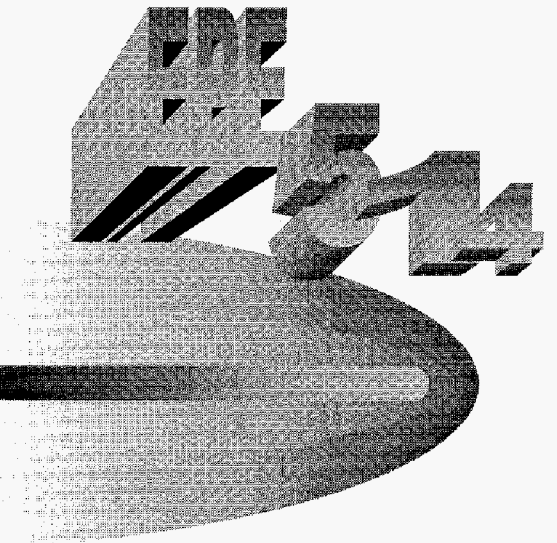
Definitive results were found on six suspect problem areas submitted for analysis.

**JET PROPULSION LABORATORY**  
**Electronic Parts Engineering Office**

	Circuit Side Scan	Non-Circuit Side Scan
Type I Delamination: Encapsulant/Die Surface		
Type II Delamination: Die Attach Region		
Type III Delamination: Encapsulant/Substrate (Die Side)		
Type IV Delamination: Substrate/Encapsulant (Backside)		
Type V Delamination: Encapsulant/Lead Interconnect		
Type VI Delamination: Intra-laminate (Laminate Substrates Only)		
Type VII Delamination: Heat Sink/Substrate		

IC defect  
descriptions are  
now identified in  
**J-STD-035**  
(Acoustic Microscopy for  
NonHermetic Encapsulated  
Electronic Components)

Source: Sonoscan Inc.



## **A New Failure Characterization Study is Underway Utilizing Plastic Part C-SAM Rejects**

### **Objectives:**

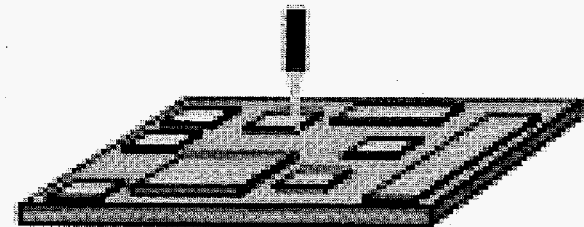
- Identify C-SAM reject parts by criteria(s)
- Measure Material Properties including sonic test, IR, X-ray
- Apply extreme temperature cycle stresses
- Repeat Material Properties Measurements including C-SAM at different intervals
- Identify all failure mechanisms and risk rate C-SAM rejects

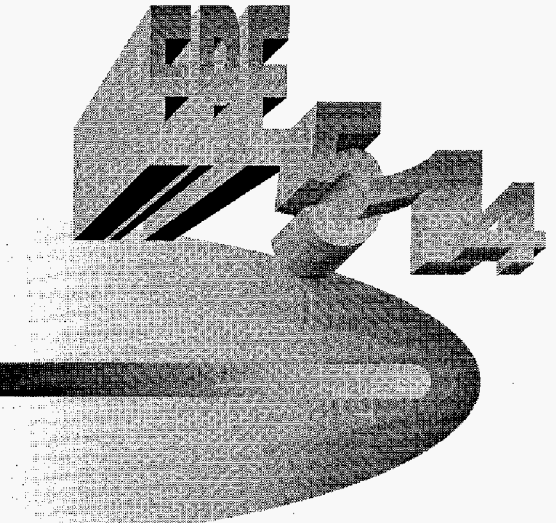


## **A Failed Chip Scale Board Assembly is under investigation utilizing C-SAM inspection on components/board**

### Objectives:

- Identify component delaminations
- Identify board layer delaminations
- Make correlation to CSP package thermal cycle failures
  - CTE Mismatch
  - Package Proximity and Location on Board
  - Ball Bond Size and Location





---

## **Summary:**

- **Some reported concerns/risks anticipated with using PEMs having evidence of delamination can be minimized and possibly eliminated with nondestructive AMI (acoustic microscopy imaging).**
- **JPL's existing screening flows for PEMs incorporates AMI 100% to enhance the reliability of parts used by JPL Projects when PEMs are the only choice available.**
- **Further investigations/studies are being conducted on individual components and board assemblies using AMI analysis. This information will provide more understanding of the correlation between delamination and component/ board failure mechanisms.**

**JET PROPULSION LABORATORY**  
**Electronic Parts Engineering Office**

*Additional information can be found at:*



<http://cots.jpl.nasa.gov>